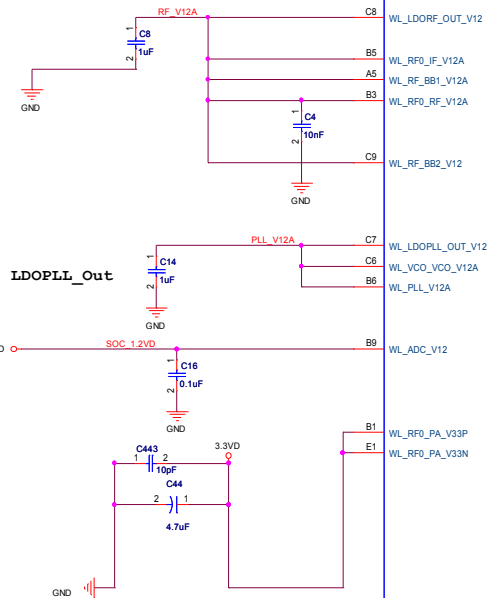
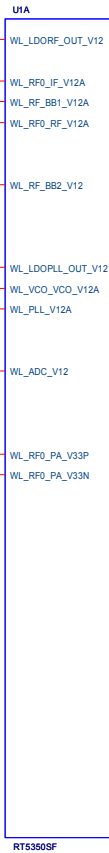


LDORF_Out

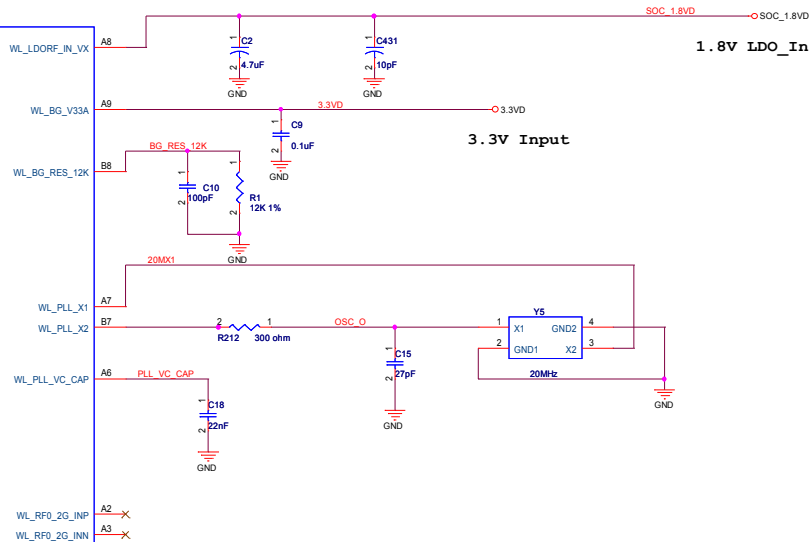
C8 layout close D8



LDOPLL_Out



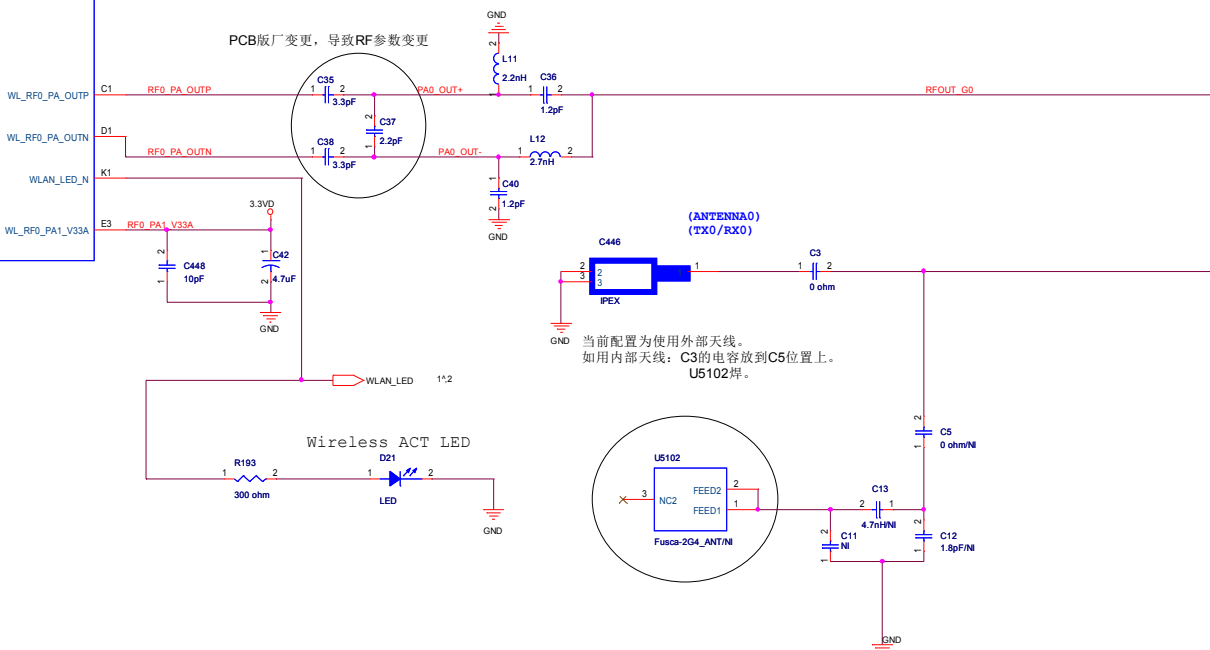
RT5350SF



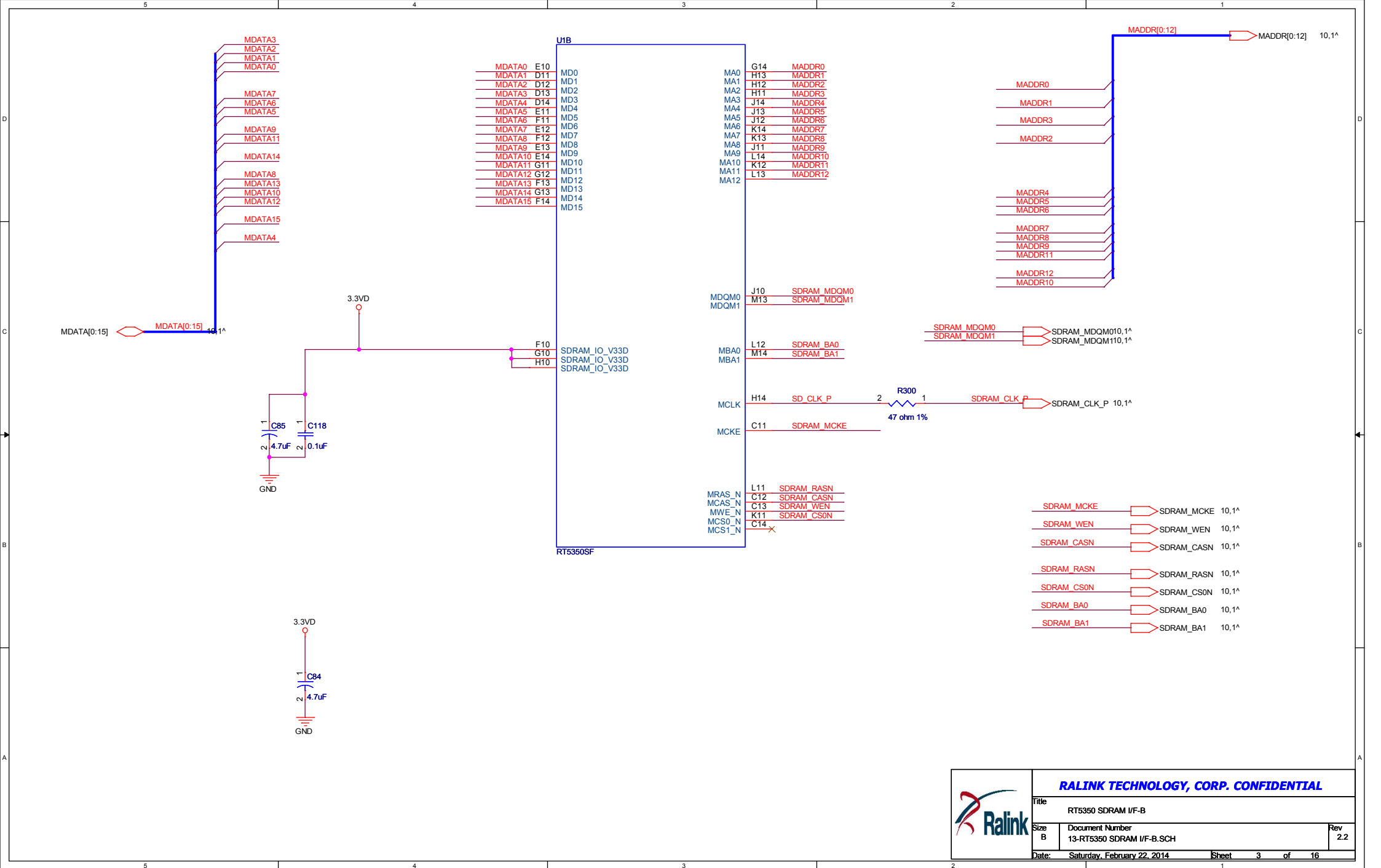
3.3V Input

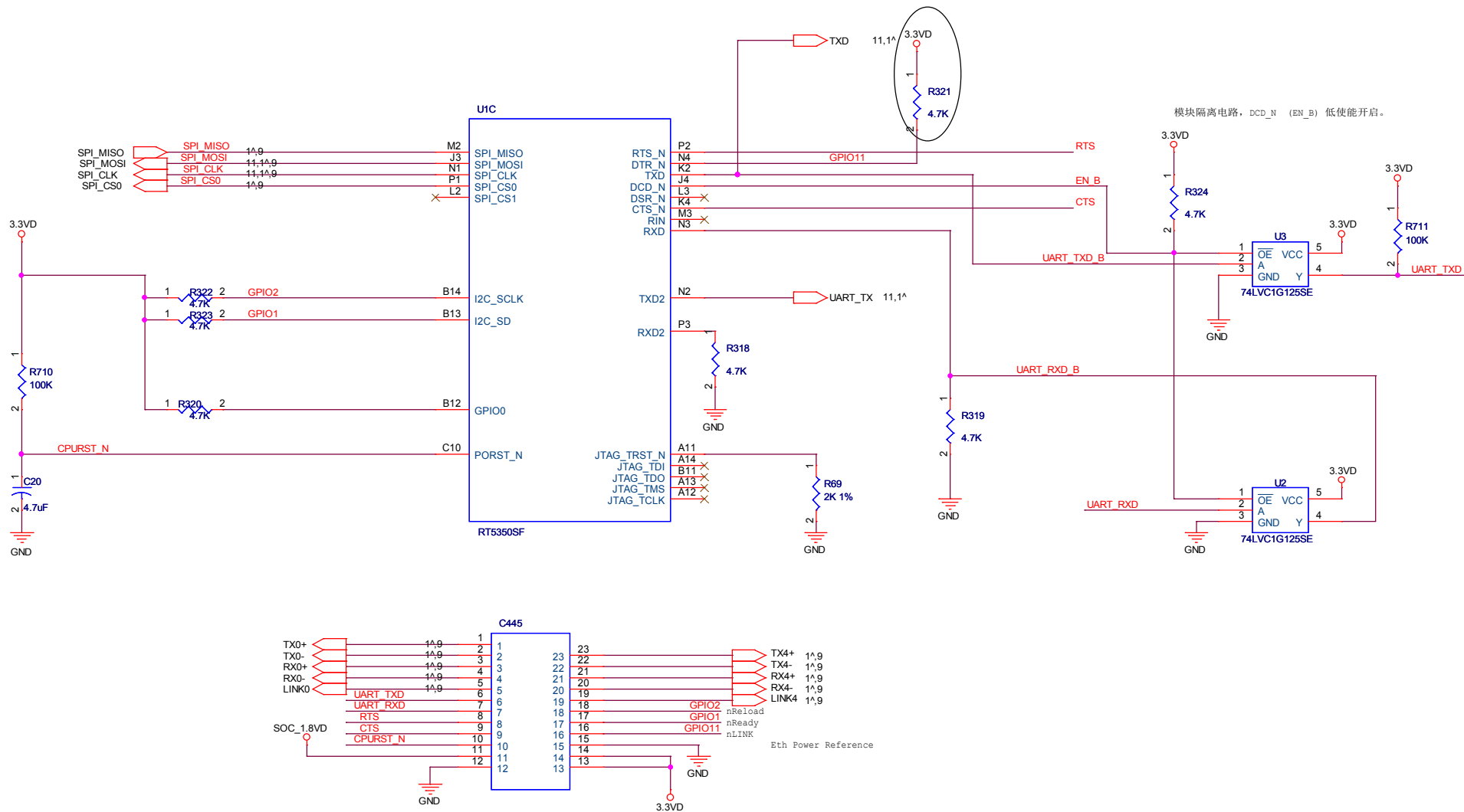
1.8V LDO_In

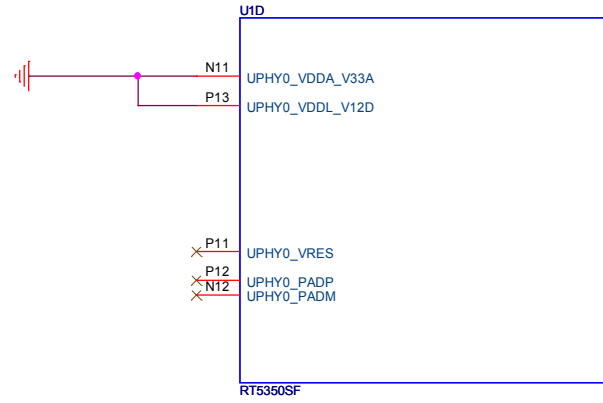
PCB版厂变更, 导致RF参数变更




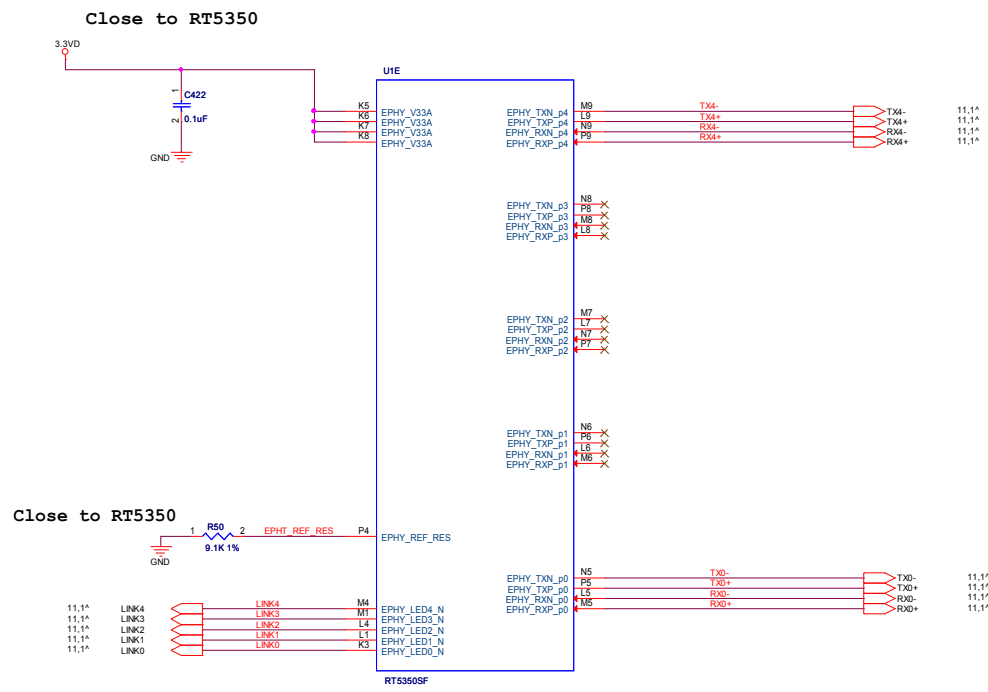
Wireless ACT LED

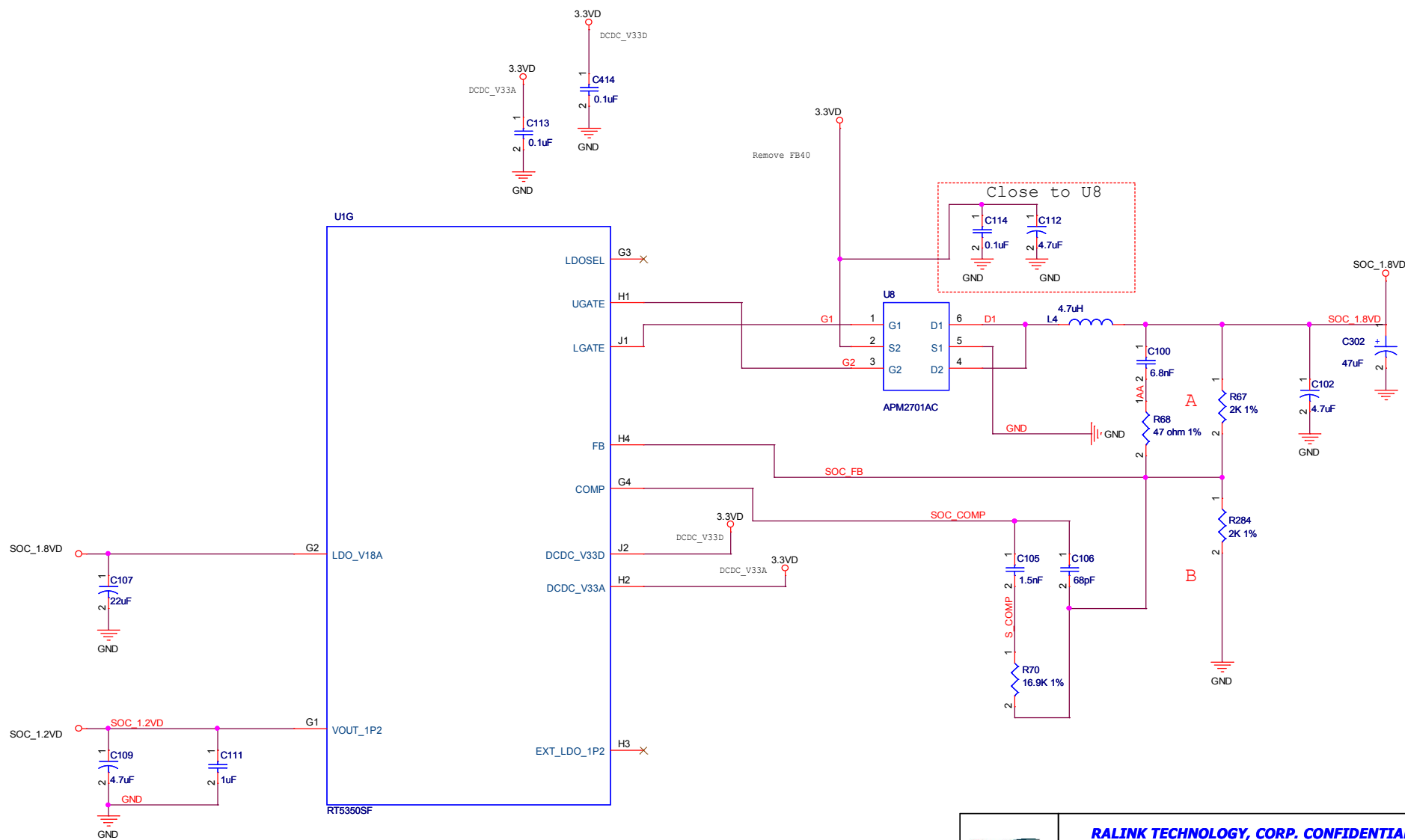


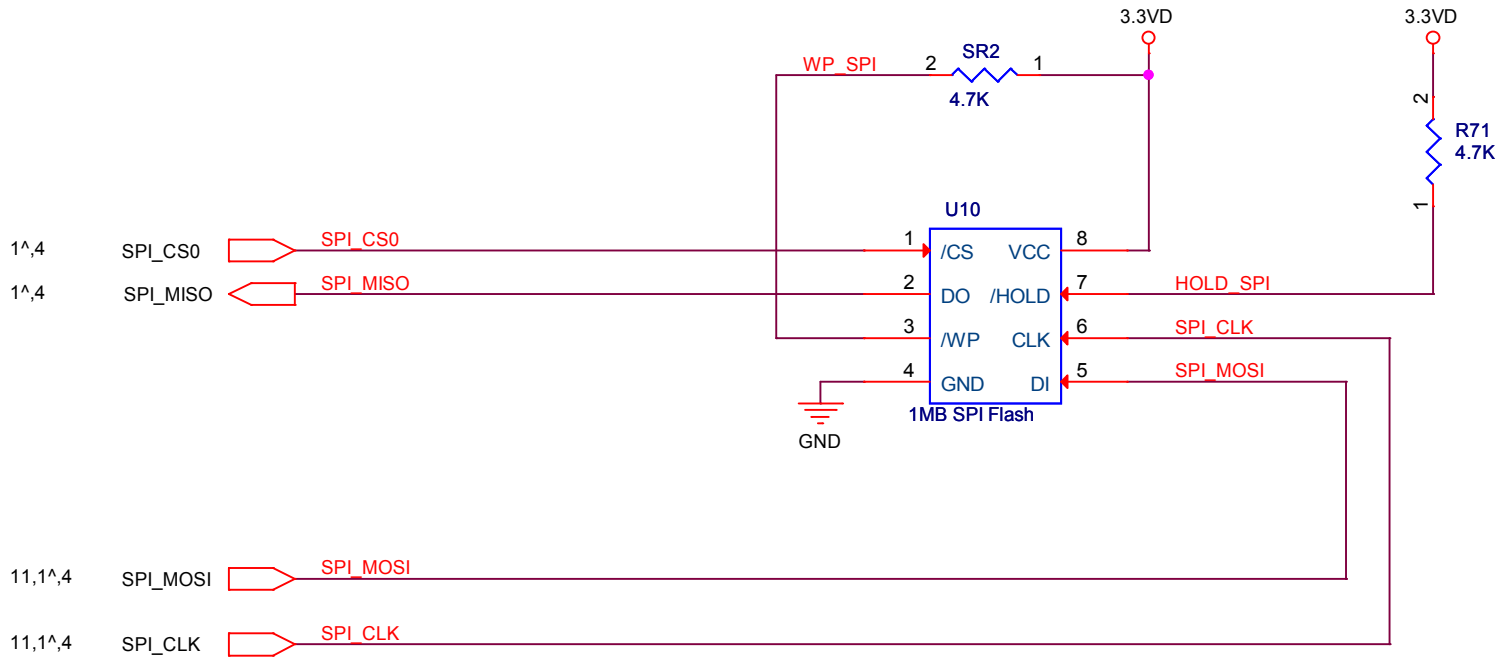




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|---|-------------------------------------|--|---------|
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| | | Title RT5350 USB-D | |
| Size B | Document Number 14-RT5350 USB-D.SCH | | Rev 2.2 |
| Date: Friday, February 14, 2014 | | Sheet 5 | of 16 |

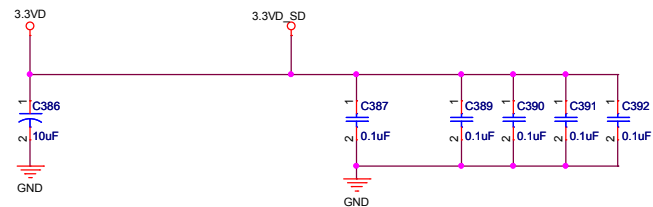
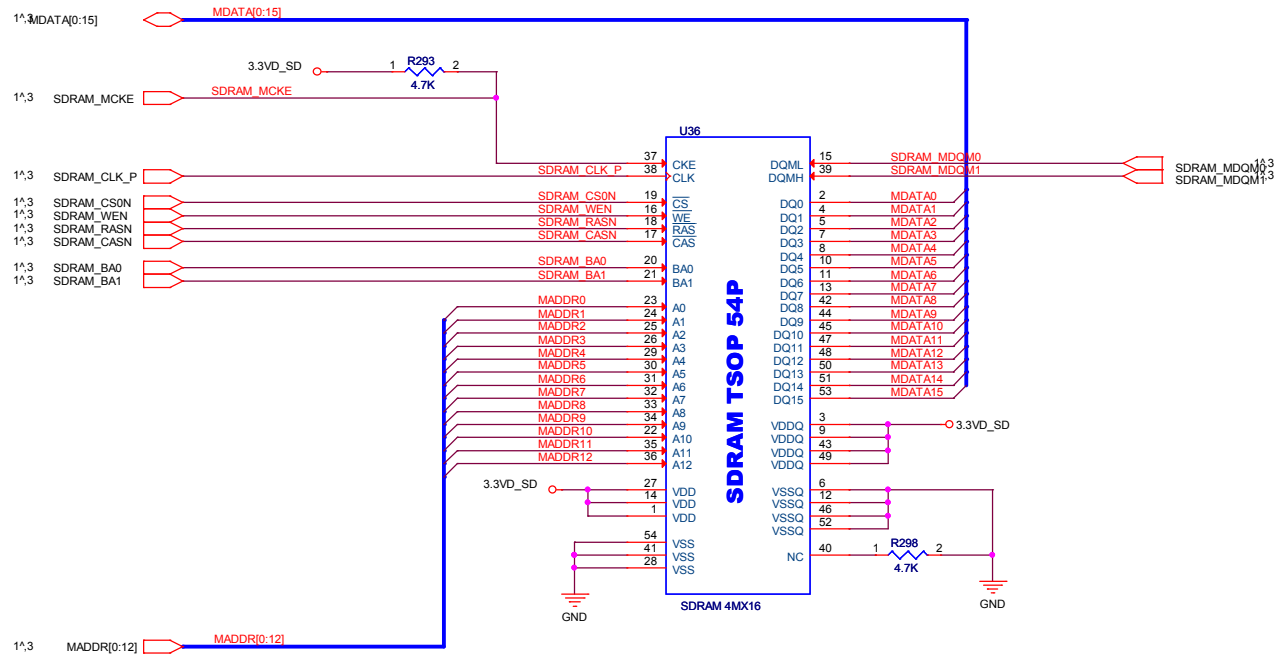


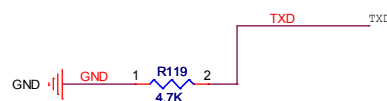
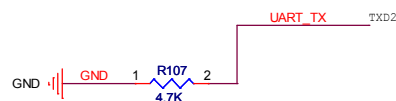
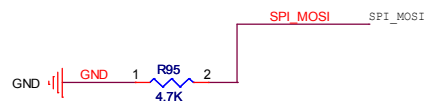
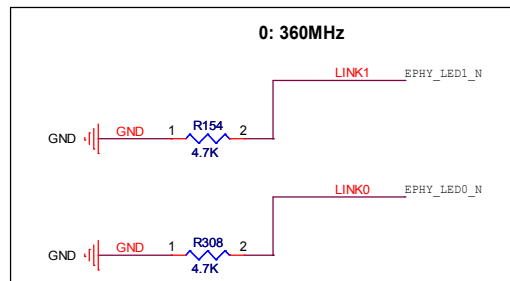
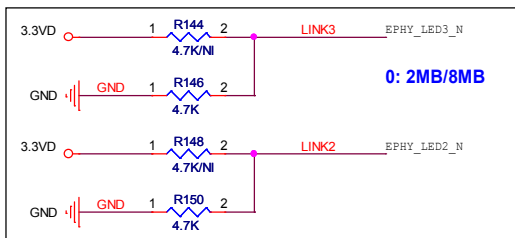
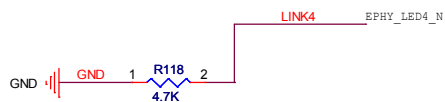
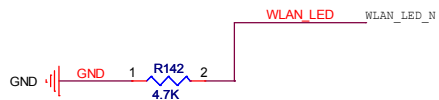
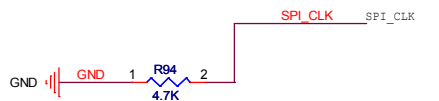
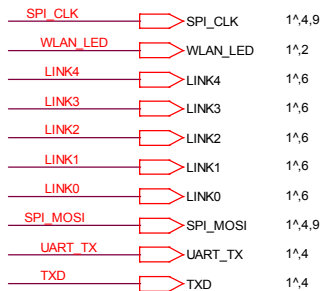




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|-------|------------------|-----|---------------------------|-------|---------|
| Title | | | SPI Flash | | |
| Size | Document Number | Rev | | | |
| A | 21-SPI Flash.SCH | 2.2 | | | |
| Date: | | | Friday, February 14, 2014 | Sheet | 9 of 16 |





RT5350 Boot Up Strapping

| Pin Name | Description | Value=0 | Value=1 |
|----------------------------|----------------|--|-------------|
| SPI_CLK | XTAL_FREQ_HI | 20MHz | 40MHz |
| WLAN_LED_N | Big Endian | Little Endian | Big Endian |
| EPHY_LED4_N | DRAM_FROM_EE | from boot strapping | from EEPROM |
| {EPHY_LED3_N, EPHT_LED2_N} | DRAM_SIZE | INIC/AP(SDR) 0: 2MB/8MB 1: 8MB/16MB 2: 16MB/32MB 3: 32MB/64MB | |
| {EPHY_LED1_N, EPHT_LED0_N} | CPU_CLK_SEL | CPU clock select 0: 360MHz 1: Reserved 2: 320MHz 3: 300MHz | |
| {SPI_MOSI, TXD2, TXD} | CHIP_MODE[2:0] | A vector to set chip function/test/debug modes 0 : Normal mode(boot fromSPI serial flash) 1 : iNIC-USB mode 2 : Reserved 3 : Reserved 4 : Reserved 5 : iNIC-PHY mode 6 : SCAN mode 7 : TEST/DEBUG mode | |